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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,378	07/13/2001	Peter Galicki	TI-29494	6116

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EXAMINER	
CHOU, ALBERT T	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/905,378	GALICKI ET AL.	
	Examiner	Art Unit	
	Albert T. Chou	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7 and 9* is/are rejected.

7)☒ Claim(s) *6,8 and 10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Scott et al. (US Patent Number: 5,796,738), hereinafter referred to as Scott.

Regarding claim 1, Scott teaches a Repeater 20 [Fig. 3; *a data routing unit*] comprising:

Uplink Modules 44 and 48 [Figs 1 & 3; col. 6, lines 43-44; *a data receiver & a data transmitter*], a plurality of Port Transceivers 54 and their associated Local Ports 46 [Figs 1 & 3; col. 6, lines 47-50; *a data receiver & a data transmitter*]; and

A Multiport Repeater 52 coupled to Uplink Modules 44 and 48 [Fig. 3; *a bridge circuit*] receives data from Port Transceiver 54 or Uplink Modules 44 and 48 and retransmits the data to all other components attached to Mulitport Repeater 52 [Fig. 3; col. 6, lines 58-60; *connected to supply data to said data receiver and to receive data from said data transmitter*].

Scott teaches message data from Data Device 22 arrive at Multiport Repeater 52 through Port Transceiver 54 / Local Port 46 [Figs 1 & 3; col. 6, lines 62-64; *said bridge circuit connected to least one data input lines*] and Multiport Repeater 52 retransmits the

data to the other Port Transceivers 54 / Local Ports 46 and both Uplink Modules 44 and 48 [Figs 1 & 3; col. 6, lines 64-65; *said bridge circuit connected to least one set of data output lines*]. Scott further teaches when Unlink Module 44 implements the bridging capability, before Uplink Modules 44 transmitting the received message data, Controller 74 reads the source and destination addresses from message data stored in Buffer 16 [Figs. 6, steps 118 & 124; col. 10, lines 11-16; *said bridge circuit responsive to a header of a data packet received from said data transmitter or received from said at least one set of data input lines*]. If the destination address is a local address, then the message is discarded from Buffer 16 [Col. 10, lines 16-20]. Otherwise, the message is transmitted over Link 58 and IRL 26 to Local Network 34 [Figs 1, 3 & 4; col. 7, lines 66-67; *to selectively route said received data packet said data to (1) said data receiver circuit, (2) a selected set of said at least one data output lines, or (3) both said data receiver circuit and a selected set of said at least one set data output lines dependent upon said header*].

Regarding claim 2, Scott teaches the Uplink Module 44 further comprises FIFOs 66 and 72 for storing data received by the receiver or data to be transmitted by the transmitter [Fig. 4; col. 7, lines 61-62; col. 8, lines 4-6; *an input/output memory connected to said data receiver storing data received by said data receiver and to said data transmitter for storing data be transmitted by said data transmitter*].

Regarding claim 3, Scott teaches that Controller 74 manages the operation of each component of Uplink Module 44. Memory 76 coupled to Controller 74 stores operational instructions and address tables for intelligent bridging and routing functions

[Fig. 4; col. 8; lines 21-25; *central processing unit connected said input/output memory storing data into said input/output memory and reading data from said input/output memory*].

Regarding claim 4, Scott teaches Repeater 20 comprising Uplink Modules 44 coupled to Local Port 42 of Repeater 16 in Local Network 34 over IRL 26 [Figs 1 & 3; col. 6, lines 43-44; *said at least one set of data input lines consists of a right set of data input lines and a left set of data input lines*], Uplink Modules 48 coupled to other repeater over IRL 30 [Figs 1 & 3; col. 6, lines 43-44; *said at least one set of data output lines consists of a right set of data output lines and a left set of data input lines*] and a plurality of Port Transceivers 54 and their associated Local Ports 46, which are able to transmit and receive the data to other ports or external devices [Figs 1 & 3; col. 6, lines 47-50; *said at least one set of data input lines consists of a right set of data input lines and a left set of data input lines and said at least one set of data output lines consists of a right set of data output lines and a left set of data input lines*].

Regarding claim 9, Scott teaches that Memory 76 coupled to Controller 74 stores address tables for intelligent bridging and routing functions [Fig. 4; col. 8; lines 21-25; *a node address register storing a uniquely assigned multibit node address*]. Controller 74 reads the destination addresses from message data stored in Buffer 16 [Figs. 6, step 124; col. 10, lines 15-16] and determines whether the destination address matches an address in the local address table stored in the Memory 76 [Figs. 6, step 126; col. 10, lines 16-18; *a node address comparator connected to said node address register for comparing predetermined destination node address bits of said header with said node*

address stored in said node address register]. If the destination address is a local address, then the message is discarded from Buffer 16 [Fig. 6, step 126, col. 10, lines 18-20]. Otherwise, the message data is transmitted over Link 58 and IRL 26 to Local Network 34 [Figs 1, 3 & 4; col. 7, lines 66-67; *said bridge circuit selectively routing said received data packet to said data receiver when said destination node address bits matches said node address*].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al. (US Patent Number: 5,796,738), hereinafter referred to as Scott, in view of Bell et al. (US Patent Number: 4,328,578), hereinafter referred to as Bell.

Regarding claim 5, Scott teaches Repeater 20 comprising Uplink Modules 44 coupled to Local Port 42 of Repeater 16 in Local Network 34 over IRL 26 [Figs 1 & 3; col. 6, lines 43-44; *said at least one set of data output lines consists of a plurality of data lines*]. Scott teaches MAC 68 reads data from buffer 66 and encodes the data [Figs. 3 & 4; col. 6, lines 62-63]. Once MAC 68 determines that Link 58 is available for transmission, it serializes the encoded data and passes this data to Encoder/Decoder

70 to translate into line level voltages. This data is transmitted over link 58 and IRL 26 to local network 24 [Figs. 3 & 4; col. 6, lines 63-67]. Scott does not expressly disclose "*a data routing unit clock line*" or "*data transmitter generating data transmitted on data lines synchronous with a transmitter clock signal on the data routing unit clock line*". Bell discloses the transceiver chassis 11 has a Master Clock 40 which produces a fixed and high frequency time signal tat is received by a Time Signal Generator 41 to generate a fixed period clock signal 100 at an output terminal 42 that is directly to the conductor 32 and multiplex circuit 43 [Figs. 2A & 2B; col. 5, lines 58-65]. Bell further teaches the clock signal 100 is utilized to coordinate timing between a transceiver chassis 43 and a microphone chassis multiplex circuit 44 wherein both of these multiplex circuits are understood to comprise controllable gating circuitry which sequentially couples an input/output terminals in accordance with received clock pulses [Figs. 2A & 2B; col. 6, lines 22-29]. It would have been obvious in Smolinske in view of Bell that in order to transmit data correctly a transmitter clock line must exist and the data transmitted on the data line must be synchronous with the transmitter clock signal.

Regarding claim 7, Scott teaches message data received from Local Network 34 over IRL 26 arrives at Encoder/Decoder 70 from Link 58 [Figs. 1 & 3; col. 8, lines 1-2; *said at least one set of data input lines consists of a plurality of data lines*]. Scott does not expressly disclose "*a data routing unit clock line*" or "*data receiver sensing data received on data lines synchronous with a receiver clock signal on the data routing unit clock line*". Gat teaches the receiver 120 and transmitter 130 connect the buffer array serial ports 111 and 113 to a transmitting medium 210 and perform standard functions

such as data encoding and clock synchronization [Fig. 2; col. 5, lines 32-35]. Bell discloses the transceiver chassis 11 has a Master Clock 40 which produces a fixed and high frequency time signal tat is received by a Time Signal Generator 41 to generate a fixed period clock signal 100 at an output terminal 42 that is directly to the conductor 32 and multiplex circuit 43 [Figs. 2A & 2B; col. 5, lines 58-65]. Bell further teaches the clock signal 100 is utilized to coordinate timing between a transceiver chassis 43 and a microphone chassis multiplex circuit 44 wherein both of these multiplex circuits are understood to comprise controllable gating circuitry which sequentially couples an input/output terminals in accordance with received clock pulses [Figs. 2A & 2B; col. 6, lines 22-29]. It would have been obvious in Smolinske in view of Bell that in order to receive data correctly a receiver clock line must exist and the data received on the data line must be synchronous with the receiver clock signal.

Allowable Subject Matter

5. Claims 6, 8 and 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert T. Chou whose telephone number is 571-272-6045. The examiner can normally be reached on 8:30 - 17:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can

be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AC
Albert T. Chou
April 4, 2005

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
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